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| **Course Title** | **Digital Logic Design** |
| **Course Code** | **CC-110** |
| **Credit Hours** | 3 (3,0) |
| **Category** | Computer Science Core |
| **Prerequisite** | None |
| **Co-Requisite** | None |
| **Follow-up** | CC-210 Computer Organization and Architecture |
| **Course Introduction** | The course introduces the concept of digital logic, gates and the digital circuits. Further, it focuses on the design and analysis combinational and sequential circuits. It also serves to familiarize the student with the logic design of basic computer hardware components. |
| **Course Description** | **Topics:** Introduction to Digital Systems, Number Systems, Introduction to Boolean Algebra, Basic theorems and properties of Boolean Algebra, Boolean Functions, Logic Gates, NAND and NOR Implementation, Representation of Function in Sum of Minterms or Product of Maxterms, Simplification of Boolean function using Karnaugh Map, Don't care Conditions, The Tabulation Method, Introduction to Combinational Logic, Design of Adders, Design of Subtractors, Code Convertors, Analysis Procedure of Combinational Circuits, Binary Parallel Adders, Decimal Adders, Magnitude Comparator, Decoders and its applications, Multiplexers, Demultiplexers, Encoders, ROM, Programmable Logic Array (PLA), Introduction to Sequential Circuits, Basic Flip Flop, Clocked RS Flip Flop, Clocked D Flip Flop, Clocked JK Flip Flop, Clocked T Flip Flop, Analysis of Clocked Sequential Circuits, State Reduction and Assignment, Flip Flop Excitation tables, Design Procedure, Design of Counters, Design with State Equations, Introduction to Registers, Shift Registers, Ripple Counters, Synchronous Counters , Timing Sequences, Memory Unit, Random Access Memory. Introduction Programmable Logic Devices (CPLD, FPGA), Lab Assignments using tools such as Verilog HDL/VHDL, MultiSim. Familiarization with Digital Electronic Trainer, Logic gates operations, Half Adder Operation, Full Adder Operation, Half Subtractor Operation, Full Adder Operation, 7-Segment Display Operation, Decoder Operation, BCD To 7-Segment Display, Multiplexer Operation, Using Multiplexer and Demultiplexer / Decoder, Multiplexing 7-Segment Displays, Comparator Operations, D Latch and Flip-Flop Operation, Latching BCD Data for Displaying On 7- Segment Display, JK Flip-Flop Operation, Random Access Memories |
| **Text Book(s)** | M. Morris Mano, Digital Logic and Computer Design, 1st Edition, Pearson, 1979, ISBN: 0132145103. |
| **Reference Material** | 2. Thomas L. Floyd, Digital Fundamentals, 10th Edition, Prentice Hall, 2008, ISBN: 0132359235.<br>3. Fundamental of Digital Logic with Verilog Design, Stephen Brown, 2/e |